

## AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method of manufacturing a semiconductor device, the method comprising:

forming a pad oxide layer on a main surface of a substrate;

forming a polish stop layer on the pad oxide layer;

forming an opening in the polish stop layer, pad oxide layer and an opening extending into the substrate;

filling the opening in the substrate with a dielectric material forming an overburden on the polish stop layer;

planarizing the overburden;

etching to remove a portion of the dielectric material forming a step, having a height substantially equal to the height of the remaining polish stop layer, between the dielectric material and the remaining polish stop layer; and

removing the polish stop layer.

2. (Original) The method according to claim 1, further comprising:

depositing a gate electrode layer; and

patterning the gate electrode layer to form a gate electrode.

3. (Original) The method according to claim 1, wherein the polish stop layer comprises silicon nitride.

4. (Original) The method according to claim 1, wherein the dielectric layer comprises silicon oxide.
5. (Original) The method according to claim 4, comprising depositing the dielectric material by chemical vapor deposition on the polish stop layer filling the opening and forming the overburden.
6. (Original) The method according to claim 1, comprising planarizing the overburden by chemical mechanical polishing such that an upper surface of the dielectric material is coplanar with an upper surface of the polish stop layer.
7. (Original) The method according to claim 6, comprising etching to form the step of about 200Å to about 1,500Å.
8. (Original) The method according to claim 7, comprising etching to form the a step of about 500Å to about 1,000Å.
9. (Original) The method according to claim 1, comprising forming an oxide liner in the opening in the substrate before filling the opening with dielectric material.
10. (Currently Amended) A method of manufacturing a semiconductor device, the method comprising:  
  
forming a pad oxide layer on a semiconductor substrate;

forming a silicon nitride polish stop layer on the pad oxide layer;  
etching to form an opening in the polish stop and pad oxide layers;  
etching to form an opening extending into the substrate;  
depositing a layer of silicon oxide on the polish stop layer filling the opening in the substrate;

conducting a chemical-mechanical polishing such that an upper surface of the silicon oxide layer is substantially coplanar with an upper surface of the remaining polish stop layer;

etching to reduce the upper surface of the silicon oxide layer so that it is below the upper surface of the remaining polish stop layer by a distance substantially equal to the height of the remaining polish stop layer; and

removing the polish stop layer.

11. (Original) The method according to claim 10, comprising forming an oxide liner in the opening in the substrate before depositing the layer of silicon oxide.

12. (Original) The method according to claim 10, comprising:

depositing a layer of polycrystalline silicon; and

etching the layer of polycrystalline silicon to form a gate electrode.

13. (Original) The method according to claim 10, comprising etching the silicon oxide layer to reduce the upper surface to a distance of about 200Å to about 1,500Å below the upper surface of the polish stop layer.

14. (Original) The method according to claim 13, comprising etching to reduce the upper surface of the silicon oxide layer to a distance of about 500 Å to about 1,000Å below the upper surface of the polish stop layer.

15. (Original) The method according to claim 10, comprising stripping the silicon nitride polish stop layer by etching under reflux boiling of phosphoric acid at about 180°C.